Application of Prognostic Health Management in Digital Electronic Systems

Patrick W. Kalgren, Mark Baybutt,
Antonio Ginart, Chris Minnella, &
Michael J. Roemer
Impact Technologies, LLC
200 Canal View Blvd.
Rochester, NY 14623
(585) 424-1990
patrick.kalgren@impact-tek.com

Thomas Dabney
Joint Strike Fighter Program Office
Suite 600, Crystal Gateway Four
1213 Jefferson Davis Highway
Arlington, VA 22202-4316
(703) 601-5619
tom.dabney@jsf.mil

Abstract— **Development of robust prognostics for digital electronic system health management will improve device reliability and maintainability for many industries with products ranging from enterprise network servers to military aircraft. Techniques from a variety of disciplines is required to develop an effective, robust, and technically sound health management system for digital electronics. The presented technical approach integrates collaborative diagnostic and prognostic techniques from engineering disciplines including statistical reliability, damage accumulation modeling, physics of failure modeling, signal processing and feature extraction, and automated reasoning algorithms. These advanced prognostic/diagnostic algorithms utilize intelligent data fusion architectures to optimally combine sensor data with probabilistic component models to achieve the best decisions on the overall health of digital components and systems. A comprehensive component prognostic capability can be achieved by utilizing a combination of health monitoring data and model-based estimates used when no diagnostic indicators are present. Both board and component level minimally-invasive and purely internal data acquisition methods will be paired with model-based assessments to demonstrate this approach to digital component health state awareness.** [1]

***Index Terms*— Automated reasoning algorithms, physics of failure modeling, prognostic and health management (PHM)**

ACRONYMS

AF	–	Acceleration Factors
BIT	–	Built-in Test
COTS	–	Commercial off-the-shelf
HASS	–	Highly Accelerated Lift Testing
MOSFET	–	Metal-oxide-semiconductor Field Effect Transistor
MTTF	–	Mean Time to Failure
µP	–	Microprocessor
PHM	–	Prognostics and Health Management
PoF	–	Physics-of-failure
RISC	–	Reduced Instruction Set Computer
RUL	–	Remaining Useful Life

[1] 1-4244-0525-4/07/$20.00 ©2007 IEEE.
Paper 1326 Version 3

1. INTRODUCTION

DIGITAL electronic boards are found in numerous facets of modern day life where consumers have come to depend on their reliability to operate effectively in both both professional and private endeavors. Furthermore, the commercial and military markets demand even greater reliability constraints on semiconductor manufactures where a system failure could produce catastrophic results. Diagnostic methods have been implemented in a variety of existing electronic systems (e.g. BIT), which are effective in identifying sources of malfunctions post-failure within the system; however, fail to track system usage throughout the systems' lifespan necessary when attempting to offer instantaneous health state assessments. A clear opportunity and vital need exists to improve digital electronic system health state awareness and prediction through development of PHM techniques.

The goal of proactive fault monitoring is to prevent the end user from experiencing the effects of the failure and ideally provide advanced notice of impending failure in due time to allow corrective measures to be taken prior to failure (i.e. reduce duty cycle, offload utilization, or schedule repair). Achieving this objective requires knowledge of how component-level failure manifests throughout the system and insight as to which measurands offer indication of incipient signs of failure. In this paper, the authors illustrate how cradle-to-grave health state awareness can be achieved through the teaming of model-based assessments in the absence of fault indications and a data driven approach used to track indicators of failure providing failure mode classification. Test results from accelerated testing of a CMOS device are presented as a basis to indicate the ability to capture fault indicators indicating impending failure and track the degradation of performance measurands. The application of complementary prognostic techniques such as physics-based component damage accumulation/aging models based on projected operating conditions, empirical (trending) models, and system level failure progression models are discussed as providing a solid foundation on which to develop

Report Documentation Page

Form Approved
OMB No. 0704-0188

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED
2007		**00-00-2007 to 00-00-2007**

4. TITLE AND SUBTITLE	5a. CONTRACT NUMBER
Application of Prognostic Health Management in Digital Electronic Systems	5b. GRANT NUMBER
	5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S)	5d. PROJECT NUMBER
	5e. TASK NUMBER
	5f. WORK UNIT NUMBER
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) **Impact Technologies LLC,200 Canal View Blvd,Rochester,NY,14618**	8. PERFORMING ORGANIZATION REPORT NUMBER
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)
	11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited

13. SUPPLEMENTARY NOTES

14. ABSTRACT
see report

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			
unclassified	**unclassified**	**unclassified**	**Same as Report (SAR)**	**9**	

which to develop verifiable prognostics assessment.

The ultimate implementation of the technology developed under this program will provide a comprehensive and effective diagnostic/prognostic solution, requiring minimal sensor retrofitting or hardware modifications, suitable for deployment on wide-ranging applications across the multiple facets of digital electronics including integration into digital electronic boards residing in COTS embedded computer system, industrial or commercial computing platforms, or adding capabilities to automated test equipment.

2. DEVICE RELIABILITY

The reliability throughout the lifespan of a population of devices is commonly illustrated through the familiar "Bathtub Curve", shown in Fig 1. The curve coveys an initially high, yet decreasing rate of failure, at the conception of the device due to anomalies in manufacturing process, handling or installation defects. Manufactures generally perform "burn-in" tests or HASS to purge the population of the units prone to premature failure; doing so advances the remaining population to the "useful" life stage where failures still occur, yet at a low and assumed to be constant rate. The final phase of life, referred to as the wearout stage, occurs when time-dependent environmental, electrical or mechanical stress age the physical properties of the device past nominal operation limits increasing the likelihood of failure amongst the remaining population.

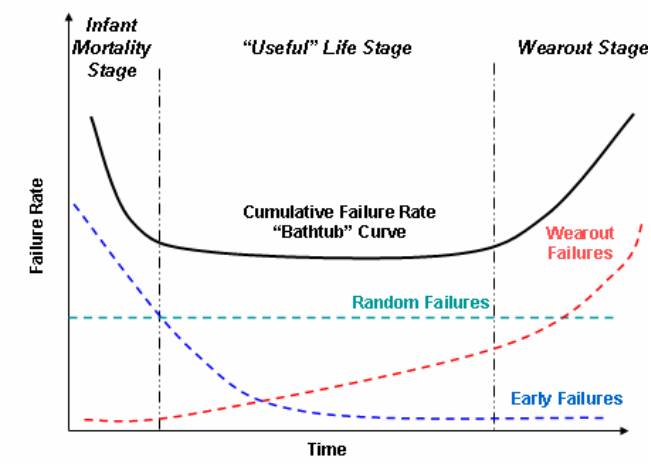


Fig 1: Device Reliability illustrated through the "Bathtub" Curve

Analysis of failures throughout the lifespan identifies numerous failure mode possibilities triggered by various failure mechanisms. A **failure mechanism** is defined as the physical phenomenon causing the onset of failure; common examples in mechanical systems are vibration, corrosion, high friction, etc. The underlying failure mechanism becomes evident to the user through **failure modes** which are tangible observations of how the system or device failed; for example for example overheating, unexpected shutdown, and reduced performance are observable failure modes. Commonly, single failure modes can be attributed to multiple failure mechanisms.

The approach presented herein identifies specific failure mechanisms prevalent in triggering failure throughout the "useful" and wearout stages of life. Accelerated aging techniques were selected and applied to test articles to increase the likelihood of failure due to the desired failure mechanism. The devices tested were verified as successfully passing "burn-in" procedures performed by the manufacturer aimed at decreasing the likelihood of early onsets of failure, thereby shifting the sampled population towards the "useful" life stage. Fig 2 illustrates the concept of multiple sources of failure modes, randomly distributed in time and normally distributed in contribution to failure rate, vertically amalgamating to the constant failure rate assumed throughout normal life. Through selectively applying accelerated aging techniques, targeting individual underlying failure mechanisms, individual failure modes may be investigated by pushing the device towards the wearout phase of life enabling observation of system level responses and performance degradation as the end of life approaches. These characteristic changes as the device transitions from useful life to end of life are of most interest when attempting to identify, classify, and track incipient signs of impending failure.

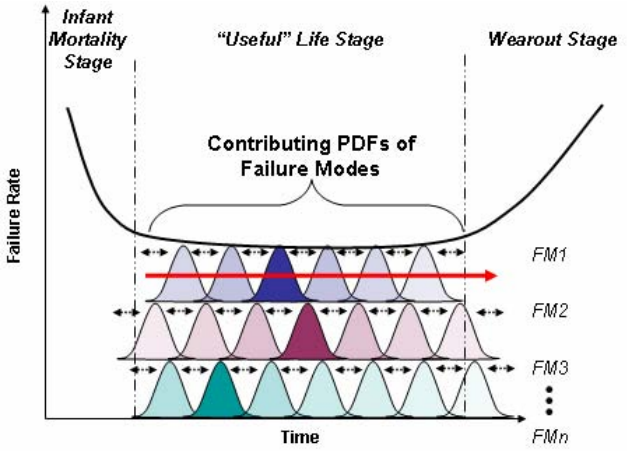


Fig 2: Contribution of Multiple Failure Modes to Device Reliability

3. DIGITAL DEVICE FAILURE MECHANISMS

The realm of digital devices is vast, spanning devices from FPGAs and DSPs to general purpose processors and certain forms of volatile and non-volatile memory. Despite functional and topological dissimilarities, all digital devices share a common functional dependence on semiconductor devices, specifically transistors. Moreover, MOSFETs are ubiquitous in digital electronics accounting for close to 99% of the FET market [1]. Thus, understanding the physics-of-failure at the transistor device level is paramount when attempting to

attempting to quantify failure modes and mechanisms within digital systems.

Devices are continually subjected to aging through electrical, mechanical and environmental stresses inherent to operational conditions throughout a given lifetime. Development of physics based diagnostic and prognostic analyses of the device or system health status is possible if knowledge of the time-dependant effects of these aging processes can be determined. Documented semiconductor PoF models can be used as a basis to derive system level models describing the tendencies and responses of the system as it reacts over time to the environmental conditions present. There are four main semiconductor failure mechanisms that contribute to aging tendencies of MOSFET devices:

1. Thermal cycling
2. Electromigration
3. Hot carrier effects
4. Time-dependent dielectric breakdown

The vast majority of semiconductor devices are based on silicon fabrication; however the following failure mechanisms can be extended to other materials such as silicon-germanium, gallium arsenide, and silicon carbide providing a powerful foundation to analyze virtually all digital devices.

A. *Thermal Cycling*

Thermal cycling is one of the main environmental acceleration factors that produce MOSFET aging. Device degradation occurs because thermal cycling deteriorates the thermal circuit which allows the device to release generated heat.

When a device composed of multiple materials, such as an IC, is exposed to the stress of thermal cycling, it deteriorates until a fracture or void space is produced (see Fig 3). Dissimilar materials are used to produce the heat transfer path to release heat generated by a functioning semiconductor device. In general, these materials have different coefficients of thermal expansion that make the device more susceptible to cracks or fractures due to the forces originated by thermal expansion and contraction. These fractures among different materials deteriorate the functionality of the device, but do not directly interfere with the software operation of the device.

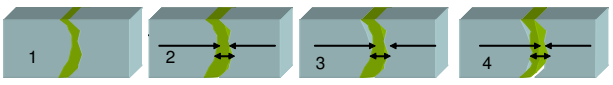


Fig 3: Void Area Creation Process Due to Thermal Cycling

The cracks caused by thermal cycling compromise the semiconductor's ability to transfer heat. The reduction in conduction ability does not destroy the semiconductor itself, but accelerates the aging process for other failure mechanisms.

Damage caused by thermal cycling accumulates every time a device experiences a power-up and a power-down cycle. Thermal cycling eventually weakens metallic contacts, triggering the occurrence of gate-oxide breakdown or contact migration. The Coffin-Manson model, shown below, can be used to estimate the number of thermal cycles before failure for a specific device.

$$N_f = C_0 \cdot (\Delta T - \Delta T_0)^{-q} \quad \textbf{(1)}$$

N_f = Number of cycles to failure
C_o = Material- Dependant Constant
ΔT = Entire Temperature Cycle
ΔT_o = Cycle in the Plastic region
q = Material–Dependant Constant (see Table 1)

TABLE 1: COFFIN-MANSON COEFFICIENTS

Material	**q**
Ductile metal (solder)	1-3
Hard metal alloys (Al-Au)	3-5
Brittle fracture(Si and Dielectrics)	6-9

B. *Electromigration*

Electromigration is the mass transport of the metal due to momentum transfer between the conducting electrons and the diffusing metal atoms. This phenomenon was observed and defined in metals, but can also be related to highly doped semiconductors (with negative thermo impedance). The 50th percentile time to failure due to electromigration is calculated using the equation given below.

$$t_{50} = A_0 \cdot j^{-2} \cdot e^{\frac{E_a}{kT}} \quad \textbf{(2)}$$

A_o = Constant
J = Current density
E_a = -0.1 to 0.2eV
T = Temperature in K
k = Boltzmann's constant

C. *Hot Carrier Effects*

As MOSFETs begin to age, the dielectric material of the device begins to degrade. The silicon dioxide (SiO_2) bonds of the dielectric break as a result of interaction between highly charged electrons, also known as hot carriers. This phenomenon is very important in MOSFET technology where the presence of high electric fields facilitates the creation of hot carriers, as shown in Fig 4.

The four common hot carrier injection mechanisms are [2]:

1. Drain avalanche hot carrier injection (DAHC)
2. Channel hot electron injection
3. Substrate hot electron injection
4. Secondary generated hot electron injection

Drain Avalanche Hot Carrier (DAHC): This phenomenon produces the most accelerated device degradation under normal operating temperatures. This occurs when the voltage applied at the drain under non-saturated conditions is higher than the voltage applied to the gate ($V_D > V_G$). High electric fields found near the drain accelerate the carriers into the drain's depletion region.

Acceleration of the channel carriers: This phenomenon, also known as *impact ionization*, occurs when the accelerated carriers collide with Si lattice atoms, creating electron-hole pairs in the process. The displaced electron-hole could gain enough energy to overcome the electric potential barrier between the silicon substrate and the gate oxide, producing gate isolation deterioration. This leads to an increase in the gate current and a reduction in the sub-threshold voltage (V_{th}).

Substrate hot electron injection: Due to the influence of the drain-to-gate field, hot carriers are generated in the substrate. These hot carriers are injected and become trapped in the gate oxide layer, causing the same degradation as DAHC.

Secondary generated hot electron injection: The number of electrons that become trapped in the interface between doped regions grows over time modifying the threshold voltage (V_{th}) and its conductance (gm).

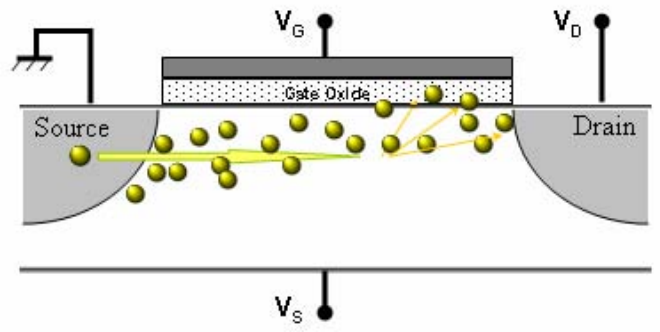


Fig 4: MOSFET Cross-sectional Visualization of Hot Carrier Effect

Independent of their origin, hot carriers produce two types of deterioration in FET technologies. The first is acceleration in time-dependant electrical breakdown of the oxide barrier (SiO_2), and the second is migration and degradation of the semiconductor.

A median time-to-failure approximation for hot carrier injection is given below:

$$t_{50} = B_0 \cdot (I)^n \cdot e^{\frac{E_a}{kT}} \quad \textbf{(3)}$$

B_o = Constant
n = 2-4
E_a = -0.1 to 0.2eV
k = Boltzmann's constant
T = temperature in Kelvin (K)
I = N-channel - peak substrate current, P-Channel - peak gate current

An example of a SiO_2 progressive breakdown in a MOSFET is shown in Fig 5.

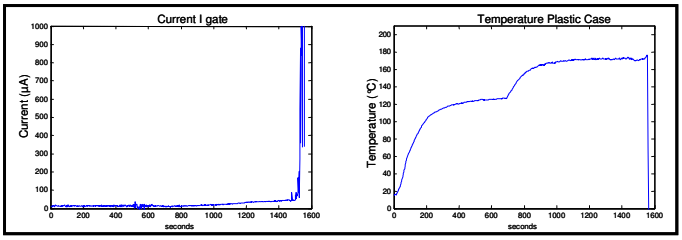


Fig 5: Gate Current Increase in an Accelerated MOSFET Aging Test

D. Time-Dependent Dielectric Breakdown

In general, time-dependent dielectric breakdown relates to the SiO_2 oxidation barrier deterioration under normal operating conditions. The reduction in life can be computed as [2]:

$$t_{50} = B_0 \cdot \left(\frac{1}{V}\right)^{(a-bT)} \cdot e^{\frac{X+\frac{Y}{T}+ZT}{kT}} \quad \textbf{(4)}$$

B_o = Constant
a = 78
b = -0.081
X = 0.759eV
Y = -66.8 eV·K
Z = 8.37E- 4 eV/K
k = Boltzmann's constant
T = temperature in Kelvin (K)
V = gate voltage

These PoF mechanisms serve as the basis for the accelerated aging processes performed on the test devices.

4. TARGET DEVICE SELECTION

An appropriate digital component or device was needed to focus the development of PHM technology upon. A range of digital component categories was considered for evaluation:

- Digital Signal Processor
- Microprocessor
- Microcontroller
- Field Programmable Gate Array
- Application Specific Integrated Circuit
- Static/Dynamic Random Access Memory (SRAM/DRAM)

While each of these digital component categories typically serves different functional purposes, they are structurally very similar. With the transistor as the common denominator, the

denominator, the component's function may have a greater influence on its susceptibility to faults than the actual architecture. For example, memory devices are regularly implemented with built-in error checking for a certain level of fault tolerance; FPGA's often run massively parallel, independent operations where a fault to a single element may have a negligible impact on the operation of the entire component. Microprocessors are a category of digital components that may be more susceptible to faults due to their complexity, large scale, and generally demanding role and responsibilities. These characteristics suggest a more significant risk associated with an undiagnosed fault in a microprocessor, and a greater need for effective PHM. In consideration of this information, the microprocessor was selected as the focus of development.

A desire to use commercially available products meeting preferred testing parameters resulted in identification of Genesi's Pegasos PowerPC computing platform. The PegasosPPC utilizes a 360 CBGA MPC7447 processor on an affordable and completely removable edge card which inserts into a fully populated motherboard (see Fig 6). The MPC7447 host processor is a high-performance, low-power 32-bit implementation of the PowerPC RISC architecture with a full 128-bit implementation of Freescale's AltiVec™ technology [7]. It has a robust data processing core incorporating a powerful 128-bit vector processing unit, double-precision floating-point arithmetic unit, superscalar data bus architecture, and sizable on-chip L2 cache memory. The capabilities of the MPC7447 are representative of processors commonly used in military, commercial and private digital systems thus an ideal point of origin for digital PHM development.

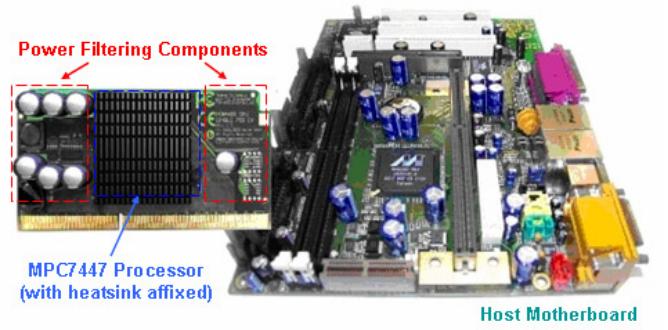


Fig 6: Processor Test Platform

One attractive feature of this product lies in the separability of the processor from its supporting circuitry (e.g. north/south bridge, interface controllers and memory). The power filtering components accompanying the processor on the edge card, shown in Fig 6, were easily removed and replicated on an intermediary board. Isolating the processor in such a manner facilitated a primary objective of focusing accelerated aging exclusively on the processor itself thereby increasing the likelihood that end-of-life system failure would originate within the processor.

5. ACCELERATED FAILURE TESTING

Operating conditions that exceed specified conditions are commonly referred to as acceleration factors. Electrical AF depend on device parameters such as voltage and current whereas mechanical AF depend on the geometry or packaging of a device, or the mechanical stress on solder joints and metal interconnects. The remaining AF may depend on environmental conditions, such as ambient temperature, external electromagnetic interference, humidity, or radiation and are known as environmental AF. The accelerated failure testing performed introduced specific electrical and mechanical stresses into the system. By subjecting the µP to elevated operating conditions outside the specified operating range, accelerated aging rapidly advanced the µP through its normal operational lifespan to the wearout phase ultimately leading to observable failure.

The following three variants of accelerated tests were performed:

1. Thermal Oscillation
2. Combinational Environment
3. Thermo-Electrical Stress

A. *Thermal Oscillation*

A µP daughtercard was placed in a programmable thermal chamber (see Fig 7) where the temperate was oscillated between preset limits with one hour cycle time to maximize the number of cycles performed per day. The temperature extremes employed for thermal cycling tests were extended beyond the minimum and maximum specified device storage temperatures (-55°C and +150°C) [7]. Baseline tests were conducted before and after cycling due to the impracticality of operation with the motherboard while in the chamber.

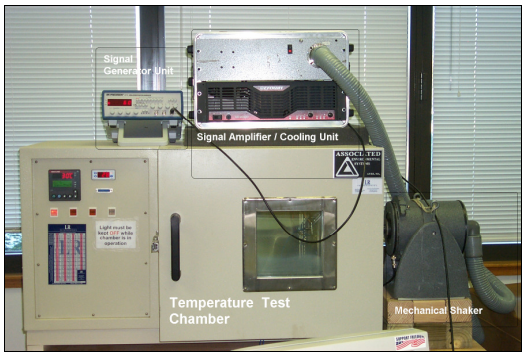


Fig 7: Environmental Test Chamber used for Thermal Oscillation and Thermal with Vibration

B. *Combinational Environment*

A µP daughtercard was secured to a custom vibration fixture (see Fig 8) connected to an electro-dynamic shaker and installed into the thermal chamber. The µP daughtercard was subjected to a fixed frequency sine wave vibration, imperially

imperially tested to induce maximum response (i.e. natural frequency), while simultaneously being subjected to identical thermal cycling as described above.

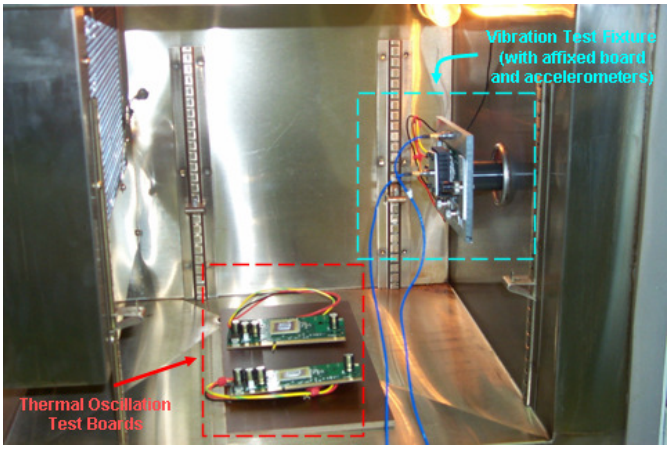


Fig 8: Internal View of Environmental Test Chamber

C. *Thermo-Electrical Stress*

The power supplied to the µP under test was switched from the motherboard ATX supply to a variable linear benchtop supply. A µP daughtercard was operated normally with the motherboard while the variable external supply applied the necessary core power to the processor while the motherboard continued to source power from the ATX supply. By isolating the processor power from the motherboard power, control over the aging profile of the processor was achieved. Once nominal operating conditions were established, the voltage was increased allowing the µP to operate at voltages beyond operational limits. The initial voltage for the thermo-electrical accelerated failure test was selected to coincide with the maximum operating voltage and temperature (1.6V and 100°C, respectfully) specified by [7]. The standard heat sink was removed and a 120 cfm fan was focused on the µP to maintain a nominal temperature of 100°C as subsequent trials progressed. Separate trials were conducted restricting and unrestricting the die temperature as the core voltage was increased.

6. TESTING RESULTS

Impact developed a suite of test algorithms in a Linux operating environment to provide baseline tests prior to and after each accelerated aging process. The test suite allowed independent and simultaneous exercise of each execution unit present within the µP (i.e. simple ALU, complex ALU, AltiVec unit, etc.), enabling analysis of functional degradation of individual operational sectors and total processor utilization. To ensure complete processor operation, the instruction fetch, memory and load/store sectors where inherently accessed when exercising execution units. In addition, the test suite provided vital control over loop iterations and number of runs allowing optimization of run time for each unit ensuring measurable performance results. Additional software was developed in the LabVIEW programming environment to measure, record and analyze test results (see Fig 9).

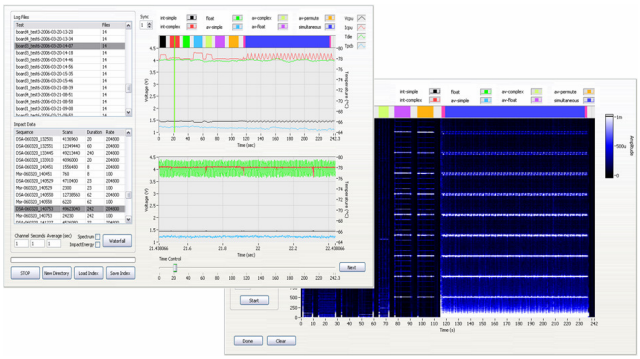


Fig 9: Data Acquisition, Logging, and Analysis/Test Suite Interface

A. *Data Analysis*

The analysis of test data from the myriad of tests performed showed a distinct ability to identify and capture incipient signs of failure prior to functional failure of the system. Moreover, the varied accelerated aging processes illustrated discernable trends in degradation progression, as shown by a comparison of Fig 10 and Fig 11, underwriting the ability to identify individual modes of failure and develop effective PHM techniques for digital systems.

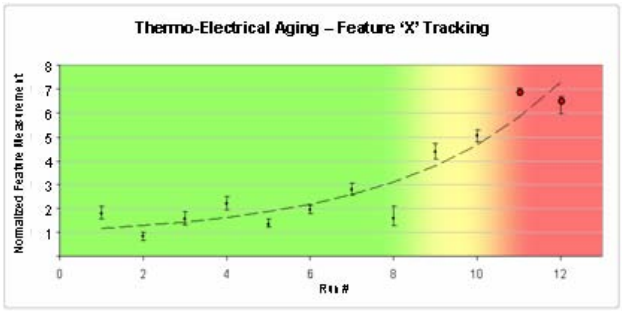


Fig 10: Feature Tracking of Thermo-Electrical Aging Process

The baseline measurements taken after successive Thermo–Electrical aging processes revealed an exponentially increasing trend in the highest fidelity feature measurement (see Fig 10). Each aging cycle escalated the core processor voltage, thereby increasing the electric field between the gate and substrate region in addition to increasing the electron mobility through the drain-to-source channel. The combination of these phenomena accelerated/excited electrons to the point of becoming trapped within the silicon dioxide (SiO_2) dielectric. This testing procedure was deemed effective in accelerating and analyzing failure modes associated with electric failure mechanisms, such as electromigration, hot carrier effect, and TDDB.

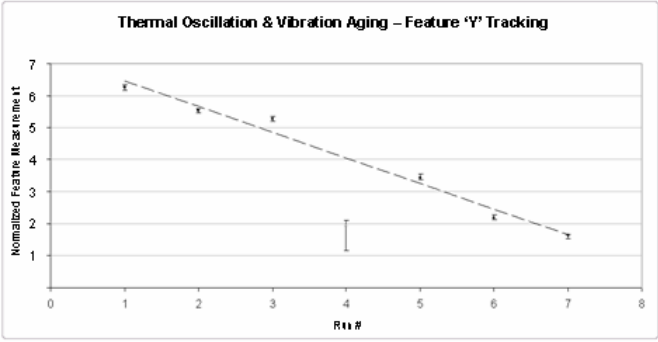


Fig 11: Feature Tracking of Thermal Oscillation & Vibration Aging Process

The compiled data extracted from each baseline test performed after every 24 hour thermal oscillation with vibration (i.e. 24 thermal cycles/test) identified a remarkably different degradation profile (see Fig 11) to that of the Thermo-Electrical aging process. The highest fidelity feature measurement specific to vibratory and thermal stress factors indicated a linear degradation as the processor aged over time. Overall, the measured data supports the proposed theory of solder joint fatigue and void area creation; as the processor under test is subjected to increasing vibratory stress, the interconnects and solder joints begin to fatigue triggering distinct failure modes, separable from those identified through electrical AF.

The results from baseline tests conducted after each series of Thermal Oscillation showed no measurable effects to the overall health of the processor. The DUT was subjected to over 400 hours of temperature oscillations beyond maximum device ratings with no discernable effect. Although Thermal Oscillation was deemed the least efficient method of accelerated aging within the allotted time frame to evoke rapid damage within the processor, Impact recognizes that thermal cycling, along with other environmental stress factors play an important role in digital systems and is continuing to pursue this type of failure progression in ongoing development endeavors.

B. Representative Life Consumption Assessment

The data acquired during Thermo–Electric accelerated life testing supports the use of the Hot Carrier Effect failure mechanism to support damage accumulated in the µP. A derivation based on the associated MTTF approximation yielded a model that effectively accounts for the life of the µP consumed as a result of time spent operating at increased temperatures. It is reasonable to expect, and indeed was demonstrated in testing, that operating a µP at temperatures significantly above those recommended reduces the life of the µP at vastly accelerated rates.

A representative model with assumed coefficients and actual test data provides an observable representation of the effects of temperature on an operating processor. The histogram displayed in Fig 12 represents the entire life of a sample µP. The vertical bars show the amount of time the µP was operated at discrete temperatures. It can be observed that extensive operation at low temperature has a largely insignificant effect on the total life of the unit. Brief periods of operation at increasingly higher temperatures consume larger and larger fractions of the unit's total life.

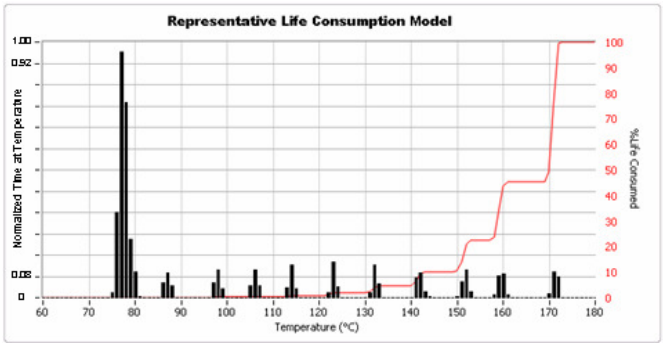


Fig 12: RUL Assessment Based Upon Modeled Feature Data

Further testing is required to empirically determine accurate approximated values as well as providing a distribution of lifetimes to use as an estimate of total life.

7. PATH FORWARD

In addition to developing system level physics of failure models, Impact Technologies is leveraging an existing Impact diagnostic/validation technology termed *SignalPro* which is capable of learning the relationships between an arbitrary set of inputs (be they features or raw sensor values) to evaluate a digital boards and its components at a system level. *SignalPro* represents a data driven condition monitoring approach to diagnostics with prognostics provided by trending.

Impact Technologies' *SignalPro* analysis engine offers a system monitoring approach that can be used to evaluate electronics system performance by employing a combination of signal processing, statistics, and data-driven modeling techniques. A complete *SignalPro* system model is created by evaluating "healthy" data during a process called training. The generated model captures the interrelationships among sensor readings or extracted features. During this training period, signal preprocessing is performed and the signal relationships and acceptable deviations are quantified.

Previously acquired historical data are captured and sent to the training engine, which finds the most efficient system representation. Statistical and correlation-based features extracted from these data further characterize the individual signal behaviors. Finally, an empirical system model is created that captures these interrelationships and the accepted deviations.

During monitoring, real-time data is used with a prediction model to assess whether the system is operating within acceptable limits. The model creates an estimate of the expected sensor values based on relationships between the new measurements and historical data. These data sets are compared to the actual data streaming in from the system, generating a residual signal. This residual signal is further analyzed to reveal unexpected (and potentially faulty) conditions.

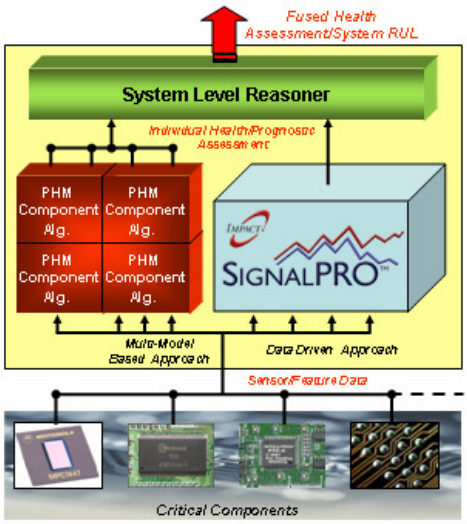


Fig 13: System Health Assessment and RUL Analysis

In addition to the data driven approach provided by the *SignalPro* analysis engine, PHM algorithms are being created for critical components within the system providing a system level model, incorporating usage based monitoring, to add prognostic assessments. The health assessments provided by each of these independent paths can then be fused at a system level reasoner to provide a high confidence analysis of the health and RUL of the electronic system, as illustrated by Fig 13.

8. CONCLUSION

The authors have shown the distinct ability to capture fault-to-failure progression data through as series of accelerated aging tests designed to isolate and increase the likelihood of failure due to specific known failure mechanisms. The matriculated failure modes were quantified through minimally invasive monitoring of system feature data as the device degraded over time. The developed understanding of semiconductor device failure and the ability to measure and trend such shifts in performance indicates the potential to develop prognostic health monitoring techniques for a wide breadth of digital components and systems.

The achievements discussed have made the first steps towards a prognostic ability for digital electronics; however, there is considerable work left ahead. Ongoing development of prognostic modeling algorithms paired with data-driven analysis, fused with reasoning methodologies, offer a viable avenue to obtain predictive insight into digital system reliability and bring PHM for digital electronics to fruition.

9. ACKNOWLEDGEMENT

This work benefited significantly from the support and technical consult of Tom Dabney of the Joint Strike Fighter program office. The work conducted was financially supported by the NAVAIR Small Business Innovative Research (SBIR) program office through a Phase I Contract (#N68335-06-C-0080).

REFERENCES

[1] J. Lau, CP Wong, JL Prince, and W Nakayama. *Electronic Packaging Design, Material, Process, and Reliability*. McGraw-Hill 1998

[2] 5th Edition Hitachi Semiconductor Device Reliability Handbook

[3] D. Brown, P. Kalgren, C. Byington, and R. Orsagh, "Electronic prognostics—A case study using global positioning system (GPS)," *IEEE AUTOTESTCON'05 Conf.*, Sept. 2005.

[4] D. Brown, P. Kalgren, and M. Roemer, "Electronic prognostics—A case study using switch-mode power supplies (SMPS)," *IEEE AUTOTESTCON'06 Conf.*, Sept. 2006.

[5] S Jayanth, J. Pradip "The case for lifetime Reliability-Aware Microprocessors" ISCA-04, June 2004

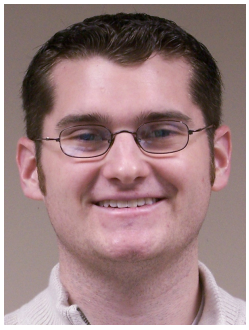
[6] K. C. Gross, S. Wegerich, and R. M. Singer, "New artificial intelligence technique detects instrument faults early," *Power Magazine*, vol. 42, no. 6, pp. 89-95, 1998.

[7] R. Singer, K. Gross, J. Herzog, R. King, S. Wegerich, "Model-based nuclear power plant monitoring and fault detection: Theoretical foundations," *Proc. Intelligent System Application to Power Systems Conference*, pp. 60-65, July 1997.

[8] S. Wegerich, A. Wilks and R. Pipke, "Nonparametric modeling of vibration signal features for equipment health monitoring," *Proc. IEEE Aerospace Conference*, March 2003.

[9] "MPC7457 RISC Microprocessor Hardware Specifications" Freescale Semiconductors, Doc. MPC7457EC, Rev 7. March 2006

Mr. Patrick W. Kalgren manages the Electronic Systems PHM group at Impact Technologies, leading the development of improved diagnostics and failure prediction to enable health management for electronic systems. Patrick has a systems. Patrick has a 20+year background in mechanical and electronic system analysis, diagnosis and repair. While previously employed by PSU ARL, Patrick researched automated classifiers and developed performance tests to assess cross data type performance. At Impact, he has developed advanced signal processing, applied AI techniques to fault classification, researched advanced database design and supervised various software projects related to vehicle health management. Patrick has a B.S. degree in Computer Engineering from Penn State University and is a member of Tau Beta Pi, IEEE, The IEEE Standards Association, and the IEEE Computer Society.



Mr. Mark Baybutt is a Project Engineer at Impact Technologies and has contributed and taken on lead roles in many projects within the Electronic Prognostic group. Mark has presented electronic diagnostic/prognostic papers in domestic and international conferences, most recently at the Symposium on Prognostics and Health Management hosted by the MIRCE Akademy, Woodbury Park, UK. As a student at the Rochester Institute of Technology (RIT), Mark co-founded and was successful in orchestrating a student lead team to the semi-final round of the DARPA Grand Challenge, a competition to develop a ground-based autonomously controlled vehicle. Mark is currently pursing his B.S. in Electrical Engineering at RIT.